AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listing, of claims in the application:

Listing of claims:

1. (ORIGINAL) A method of fabrication of doped regions in a semiconductor device; comprising the steps of :
   a) providing a {001} silicon substrate;
   b) forming a gate over said silicon substrate; said gate having a width and a length; a channel under the gate; said channel having a channel direction parallel with the direction of said gate width; said channel direction is [100] or [010] direction;
   c) implanting ions into said silicon substrate to form a doped region adjacent to said gate; the implantation of ions comprises a large angle tilt implant with a twist of between about 40 and 50 degrees and a tilt angle of 40 and 50 degrees.
2. (ORIGINAL) The method of claim 1 wherein said doped region is a N- LDD in an offset LDMOS FET.
3. (PREVIOUSLY PRESENETED) The method of claim 1 wherein said ions being implanted about along the |110| directions of the silicon substrate.
4. (PREVIOUSLY PRESENETED) The method of claim 1 wherein the implanting of said ions is performed in one implant step at an about 45 degree twist implant and a tilt angle of about 45 degrees.
5. (PREVIOUSLY PRESENETED) The method of claim 1 wherein said silicon substrate has a notch/flat at a |110] direction.
6. (CURENTLY AMENDED) The method of claim 1 wherein the implanting of ~~ion~~ ions further comprises: said silicon substrate has a notch/flat at a <110> direction,

   the implantation comprises an implant with a 45 tilt and 45 twist and the ions enter the substrate aligned at a <0 -1 -1> direction whereby the direction increases the channeling.

7. (PREVIOUSLY PRESENETED) The method of claim 1 wherein said channel has an annular shape with a doped region on the inside of said channel and a second doped region surrounding the outside of said channel.

8. (PREVIOUSLY PRESENETED) The method of claim 1 wherein said channel has an annular shape with a doped region on the inside of said channel region and a second doped region surrounding the outside of said channel;

and the implanting of said ions further comprises a quadra implant at the twist angles of about 45, 135, 225 and 315 degrees with a range of +/- 5 degrees; and a tilt angle between 40 and 50 degrees.

9. (PREVIOUSLY PRESENETED) The method of claim 1 wherein said channel has an annular shape with a doped region on the inside of said channel and a second doped region surrounding the outside of said channel region;

and the implanting of said ions further comprises a quadra implant with the ion beams aligned with the <110> direction within plus/minus 2 degrees.

10. (PREVIOUSLY PRESENETED) The method of claim 1 which further includes forming a High Vt NMOS FET from said gate and doped regions.

11. (PREVIOUSLY PRESENETED) The method of claim 1 wherein a LDMOS device is formed.

12. (PREVIOUSLY PRESENETED) The method of claim 1 which further comprises forming a second gate over said silicon substrate; said second gate having a width and a length; a second channel under the second gate; said second channel having a second channel direction parallel with the direction of width of said second gate; said second channel direction is parallel or perpendicular with the <110> direction.

Claims 13 to 39 (Canceled)

40. (NEW) The method of claim 1 wherein the implanting of ions further comprises:

the implantation comprises an implant with a 45 tilt and 45 twist and the ions enter the substrate aligned at a <0 -1 -1> direction whereby the direction increases the channeling.